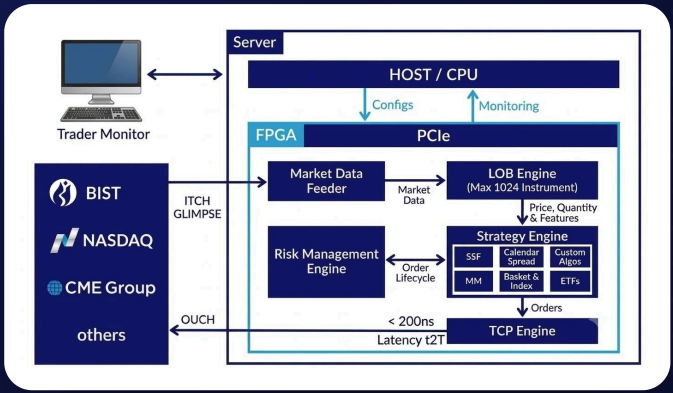
FULL FPGA

Matriks Full FPGA HFT and Market Making Platform

End-to-end hardware, ultra-low latency.

From the moment market data arrives on the wire until the order reaches the exchange, the entire critical path runs on a single FPGA chip. The operating system, drivers and CPU queues are taken out of the loop, leaving predictable, nanosecond-level execution.



<200 ns
Tick-to-Trade
End-to-end, 148 ns average

<70 ns
LOB Update
Order book build

1024
Instruments
Tracked concurrently

256
Strategy Pairs
Per strategy

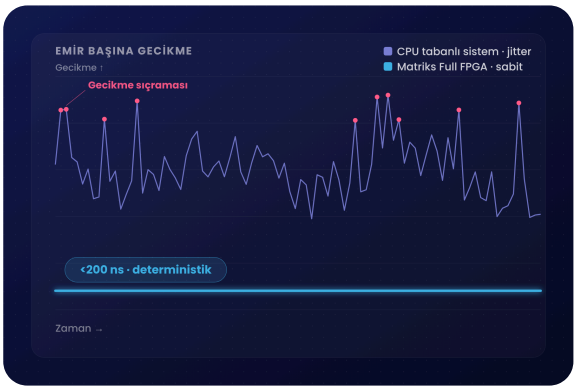
6.2 ns
Order Packing
OUCH in hardware

0
Jitter
Deterministic operation

WHY FULL FPGA?

Go beyond the limits of traditional systems

CPU-based trading systems suffer jitter of microseconds or even milliseconds due to operating-system interrupts and processor queues. In volatile moments, that delay means missed opportunities and higher risk.



PROBLEM

Operating System Layer
Interrupt latency and context-switching overhead

PROBLEM

CPU Queues
Unpredictable latency under variable load

SOLUTION

Full FPGA
The CPU leaves the critical path; every operation completes in the same, deterministic time

Speed
Nanosecond-level end-to-end execution

Determinism
Zero jitter, predictable performance

Safety
Hardware risk checks and limit management

Integration
Easy PCIe management and real-time reporting

HOW IT WORKS

Zero CPU, fully hardware data path

1

Market Data In

ITCH / GLIMPSE data is parsed in hardware and the order book is updated instantly.

< 70 ns

→

2

Hardware Decision

The strategy engine processes best prices; the risk engine checks limits in the same clock cycle.

Deterministic

→

3

Order Out

The OUCH order is built in hardware and sent straight to the exchange by the on-chip TCP engine.

Total < 200 ns (avg. 148 ns)

PLATFORM MODULES

An end-to-end trading pipeline on a single chip

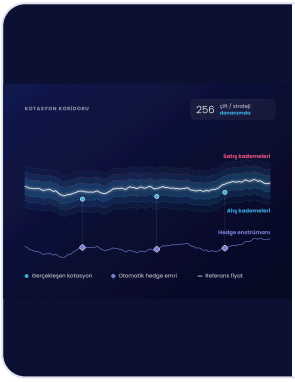


LOB ENGINE

Limit Order Book Management

Full-depth order books for 1024 instruments built in under 70 ns.

- 1024 concurrent instruments
- < 70 ns book build time
- Top-N fed to strategies instantly

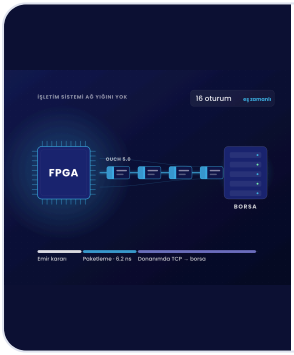


STRATEGY ENGINE

Strategies Running in Hardware

Multi-level price corridors for 256 pairs per strategy.

- Market-making strategy
- Passive risk management (auto hedge)
- Quote updates within nanoseconds



TCP ENGINE

Direct and Secure Connectivity

OUCH packets are built at NIC level within 6.2 ns.

- No operating-system network stack
- 16 concurrent sessions
- OUCH 5.0 standard



RISK & SAFETY

Risk Checks in Nanoseconds

Every order passes hardware limit checks before reaching the exchange.

- Position and net-position limits
- Sliding-window order-rate limit
- Instant block of out-of-limit orders

Strategy Library

SSF Market Making · **FaK / FoK Spread** · **Calendar Spread** · **Basket & Index** · **ETF** · **Custom Algorithms**

Custom algorithms are integrated into the modular architecture.

End-to-end latency comparison

Traditional CPU	~50 µs	
GPU accelerated	~10 µs	
Matriks Full FPGA		**<200 ns**

Up to 50× lower latency · Matriks internal measurements

MATRIKS

Built for desks where every nanosecond counts.

Contact us for a demo and detailed information.

www.matriksdata.com

Also in the HFT family: Matriks Hybrid HFT and Market Making Platform